

MILITARY SPECIFICATION

**CV7527 - 30**

SEMICONDUCTOR DEVICE, TRANSISTORS

Description:- This specification covers the detail requirements for Silicon NPN High power transistors and is in accordance with K.1007 Issue 3 except as otherwise stated.

Mechanical Dimensions and Outlines:- K.1007 Section B, 10.3.2.1 and 10.4.2.1.

Connections:- Lead 1, Base. Lead 2, Emitter. Collector connected to case.

Absolute Maximum Ratings

Device	Rating	$V_{CBO}$	$V_{EBO}$	$V_{CEO}$	$V_{CEX}$	$I_C$	$I_B$	$T_{stg}$	$T_j$	$P_C$
	Unit	V	V	V		A	A	$^{\circ}C$	$^{\circ}C$	W
CV7527 & CV7529	Min	-	-	-		-	-	-65	-	-
	Max	60	10	40	60	6	3	200	200	75
CV7528 & CV7530	Min	-	-	-	-	-	-	-65	-	-
	Max	100	10	55	100	6	3	200	200	75
	Note									B

Device	Rating	Shock	Vibration
	Unit	g	g
All	Max	1500	20
	Note	A	

Note A Duration 0.5 m sec.

B See derating curve Fig. 1 Page 11

C Commercial equivalents ZM487 - ZM490

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## Primary Electrical Characteristics

Characteristic		$I_{CBO}$	$I_{EBO}$	$V_{CE}$ (sat)	$V_{CE}$ (sat)	$V_{BE}$	$h_{FE}$	$I_{CBO}$	$f_{hfb}$
Unit		$\mu A$	$\mu A$	V	V	V		mA	Kc/s
CV 7527 & CV 7528	Min	-	-	-	-	-	15	-	500
	Max	25	25	3.0	-	3.5	45	1.0	-
CV 7529 & CV 7530	Min	-	-	-	-	-	25	-	500
	Max	25	25	-	1.0	2.5	75	1.0	-
CONDITIONS	$T_{case}$ °C	25	25	25	25	25	25	150	
	$V_{CB}$ V	30						30	12
	$V_{CE}$ V					4.0	4.0		
	$V_{EB}$ V		10						
	$I_C$ mA		0	1.5	1.5	1.5	1.5		0.10
	$I_E$ mA		0					0	
	$I_B$ mA			300	100				

Reliability Assurance Requirements:- Under Discussion

## Requirements

Marking: As K.1007 Section B. 1.3.4.

## Quality Assurance Provisions

Destructive Tests: The tests listed in Table 2, Group B Inspection, sub-group 2, 3 and 4 and Table 3 Group C Inspection, sub-group 2 are considered destructive.

Group C Inspection: This inspection shall be conducted on the initial lot and thereafter every ninety days or every fifth lot, whichever occurs first.

## Preparation for Delivery

Packaging The device shall be packed according to K.1007 Section A 1.2(c).

## Joint Service Catalogue Numbers

CV 7527 = 5960-99-037-3774  
CV 7528 = 5960-99-037-3775  
CV 7529 = 5960-99-037-3776  
CV 7530 = 5960-99-037-3777

This specification has been prepared by, and the Qualification Approval Authority is:-

Ministry of Aviation, Signals Research and Development Establishment,  
Christchurch, Hampshire, England.

TABLE 1 GROUP A INSPECTION

Examination or Test	TEST CONDITIONS		AQL %	Insp. Level	Symbol	Limits		Units
	K1007/ NATO REF.	Specific Conditions				Min	Max	
<u>SUB-GROUP 1</u> Visual and Mechanical Inspection	5.1	Excluding Physical Dimensions	0.65	I				
<u>SUB-GROUP 2</u> Collector-Base Cut-Off Current (1)	7.2.5.1	$V_{CB} = 30V$	0.65	II	$I_{CBO}$	-	25	$\mu A$
Collector-Emitter	7.2.2.2.1	$I_E = 0$ $I_C = 100mA$			$V_{CEO}$ (sus)			
Sustaining Voltage		$I_B = 0$						
Collector-Emitter	7.2.2	$I_C = 0.5 mA$			$V_{CEX}$	40	-	V
Breakdown Voltage		$V_{EB} = 1.5 V$				55	-	V
Emitter-Base Cut-Off	7.2.6	$V_{EB} = 10 V$				60	-	V
Current		$I_C = 0$				100	-	V
					$I_{EBO}$	-	25	$\mu A$

TABLE 1 GROUP A INSPECTION (contd)

Examination or Test	K1007/ NATO REF.	TEST CONDITIONS		AQL %	Insp. Level	Sym-Bol	Limits		Units
		Specific Conditions					Min	Max	
<u>SUB-GROUP 2</u> Static Forward Current Transfer Ratio	7.3.4	$I_C = 1.5A$ $V_{CE} = 4V$	CV 7527 CV 7528 CV 7529 CV 7530	2.5	I	$h_{FE}$	15 45	25 75	V
Collector-Emitter Saturation Voltage	7.3.3	$I_C = 1.5A$ CV 7527 CV 7528 $I_B = 300mA$ CV 7529 CV 7530 $I_B = 100mA$				$V_{CE} (sat)$	3.0 1.0		V V
Base-Emitter Voltage	7.3.2	$I_C = 1.5A$ $V_{CE} = 4V$	CV 7527 CV 7528 CV 7529 CV 7530			$V_{BE}$	3.5 2.5		V V
<u>SUB-GROUP 4</u> Small Signal Forward Current Transfer Ratio Cut-off frequency	7.5.1	$I_C = 100 mA$ $V_{CB} = 12V$		4.0	IA	$f_{hfb}$	500	-	Kc/s
Collector-Base Cut-Off Current (2)	7.2.5.1	$T_{amb} = 150^\circ C$ $V_{CB} = 30V$ $I_E = 0$				$I_{CBO}$	-	1.0	mA

## TABLE 2 GROUP B INSPECTION

See Page 3 Quality Assurance Provisions, Destructive Tests

Examination or Test	TEST CONDITIONS		AQL %	Insp. Level	Sym- bol	Limits		Units
	K1007/ NAIO REF.	Specific Conditions				Min	Max	
<u>SUB-GROUP 1</u> Physical Dimensions	5.1	According to drawings 10.3.2.1 and 10.4.2.1	6.5	IC				
<u>SUB-GROUP 2</u> Solderability	5.13		4.0	IA				
Temperature Cycling	5.5	-65°C to +200°C						
Moisture Resistance	5.3.1							
<u>SUB-GROUP 3</u> Vibration Fatigue	5.15	Non-operating	4.0	IC				
<u>SUB-GROUP 4</u> Omitted								
<u>SUB-GROUP 5</u> Omitted								
<u>SUB-GROUP 6</u> Omitted								

TABLE 2 GROUP B INSPECTION (contd)

Examination or Test	K1007/ NATO REF.	TEST CONDITIONS		AQL %	Insp. Level	Sym- bol	Limits		Units
		Specific Conditions					Min	Max	
<u>SUB-GROUP 7</u> High Temperature Life (non-operating)	6.2.1 6.6.1.2.2	$T_{stg} = +200^{\circ}C$ Duration = 1000 hours		4.0	I				
<u>SUB-GROUP 8</u> Operating Life	6.3	CV 7527 CV 7529 $V_{CB} = 40V$ min CV 7528 CV 7530 $V_{CB} = 55V$ min $T_{amb}$ at any single temperature between $25^{\circ}C$ and $125^{\circ}C$ with the corresponding $P_{tot}$ given by the derating curve. Fig. 1 Page 11. See Appendix A.							
<u>Post Test End Points for Sub-Groups 2, 3, 7 &amp; 8</u>									
Collector-Base Cut-off Current (1)	7.2.5.1	$V_{CB} = 30V$ $I_E = 0$				$I_{CBO}$	-	50	$\mu A$
Static Forward Current Transfer Ratio	7.3.4	$I_C = 1.5A$ $V_{CE} = 4V$ CV 7527 CV 7528 CV 7529 CV 7530				$h_{FE}$		10 20	

TABLE 3 GROUP C INSPECTION

See Page 3 Quality Assurance Provisions Group C Inspection

Examination or Test	TEST CONDITIONS		AQL %	Insp. Level	Sym-bol	Limits		Units
	K1007/ NAJO REF.	Specific Conditions				Min	Max	
<u>SUB-GROUP 1</u>								
Omitted								
<u>SUB-GROUP 2</u>			6.5	IA				
Shock	5.17.1	5 blows in each of three mutually perpendicular directions						
<u>Post Test End Points for Sub-Group 2</u>								
Collector-Base Cut-Off	7.2.5.1	$V_{CB} = 30V$			$I_{CBO}$	-	50	$\mu A$
Current (1)		$I_E = 0$						
Static Forward Current	7.3.4	$I_C = 1.5A$			$h_{FE}$			
Transfer Ratio		$V_{CE} = 4V$						
		CV 7527 CV 7528				10	-	
		CV 7529 CV 7530				20	-	



APPENDIX 'A'Inspection Level

For lot sizes up to 200, at least one transistor shall be taken from each lot and life tested for 1000 hours. For lot sizes 201 and over, at least two transistors shall be taken from each lot and life tested for 1000 hours.

Merit Life

Merit Life is defined as the ratio of the actual life hours for one or more transistors to the total life hours that would have occurred had there been no failures, expressed as a percentage:-

$$\text{Merit Life} = \frac{\text{Actual hours run}}{\text{Total possible hours}} \times 100\%$$

Classification of failures

Electrical inoperatives shall be the criterion of failure, and the life test positions shall be so arranged as to indicate a failure when it occurs. If a failure occurs, the number of hours run when the transistor was last recorded as operating shall be taken as the actual life. At the end of the 1000 hours period the same sample shall pass the post test end point limits.

Procedure of continuous production

When 1000 hours have elapsed since the sample drawn from the first lot was placed on life test, there should be at least four additional samples undergoing life test, with various numbers of hours on test. The Merit Life shall be computed for the first five lots. If the Merit Life exceeds 90% the first lot is acceptable. When 1000 hours have elapsed since the sample from the second lot was placed on life test, the merit life shall be computed using the test results from the first five lots. If this exceeds 90% the second lot is acceptable. The acceptability of the third, fourth and fifth lots is determined from the first five lots.

If when the sample from one of the first five lots have been life tested for 1000 hours, the computed Merit Life is 90% or less, the lot from which the sample was drawn shall be held in store. If when the sample from the subsequent lot has been life tested for 1000 hours, the computed Merit Life exceeds 90% both lots shall be accepted. If the Merit Life is 90% or less, both lots shall be held. When the sample from the fifth lot has been life tested for 1000 hours, if the computed Merit Life for all five samples exceed 90% all lots being held shall be accepted. If the Merit Life is 90% or less, all lots being held shall be rejected.

When the sample from the sixth lot has been life tested for 1000 hours the Merit Life shall be computed for the samples from lots 2 to 6. If this

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exceeds 90%, lot 6 shall be accepted: if it is 90% or less, lot 6 shall be rejected. A similar procedure shall apply for subsequent lots, the Merit Life being computed on the combined results of the completed life test of the lot under consideration and the previous consecutive lots.

When any sample has passed the prescribed life test period or has failed it shall be removed from test.

## Reduced Duration

When five consecutive lots have been accepted without any of them having been held due to failure to meet the 90% merit life requirement, reduced duration life testing is applicable, and the Merit Life shall then be computed after the sample from a lot has been life tested for 240 hours. If when a sample from a given lot has been life tested for 240 hours the computed Merit Life is 90% or less, the lot shall be held in store and the life test of that sample and subsequent samples shall continue to 1000 hours, the Merit Life being computed after 1000 hours for each sample. Reduced duration testing shall be again applicable after five consecutive lots have been accepted.

## Single lot or non-continuous production

If production is not continuous (see section 6.6) the above procedure cannot be used. In this case the manufacturer shall place at least five transistors on life test from a given lot. After 1000 hours the Merit Life for the sample shall be computed and if this exceeds 90% the lot shall be accepted. If it is 90% or less the lot shall be rejected.

If production is continuous (section 6.6), but an interval of more than one week occurs between any two lots at the start of a production run, either the manufacturer shall place additional transistors on life test from one or more lots, or lots shall be held in store for a period after the sample has completed 1000 hours of life test, so that the Merit Life is computed from the results of life test on not less than five transistors before a determination of acceptability is made.

## Additional samples

The manufacturer may place on life test any number of additional samples from each lot, provided the minimum requirement of 1, 2 or 5 as the case may be is met. In addition, after the life test has started for any lot, the manufacturer may add an additional quantity to the initial life test sample, but this may be done once only for any life test lot.

FIG. I.  
DERATING CURVE.

